HETEROSTRUCTURE SEMICONDUCTOR DEVICE

REFERENCE TO PRIOR APPLICATIONS

[0001] This application is related in some aspects to a commonly owned co-pending U.S. Patent Application No. 09/966,563, filed on September 27, 2001, and claims the benefit of co-pending U.S. Provisional Application No. 60/461,092, filed on April 8, 2003, both of which are hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

[0002] The invention relates generally to field effect transistors, and more specifically to a nitride-based heterostructure field effect transistor having a quaternary strain matching layer for controlling strain.

2. RELATED ART

[0003] To date, III-N field effect transistors (i.e., a field effect transistor made of elements from group III and nitrogen) such as high microwave power heterojunction field effect transistors (HFETs), metal-oxide HFETs (MOSHFETs), and metal-insulator HFETs (MISHFETs) use AlGaN/GaN heterojunctions with the two-dimensional electron gas channel formed at the AlGaN/GaN heterojunction interface. This AlGaN/GaN heterojunction design has several limitations.

[0004] For example, in the heterojunction interface, carrier confinement is achieved by a self-consistent triangular potential quantum well. However, carriers can readily spill over into the

buffer layer or the barrier layer. Such spill over increases low frequency noise and decreases transconductance. Further, carriers that have spilled over get trapped, thereby causing slow transient processes and a Radio Frequency (RF)-current collapse. Still further, a large gate voltage swing can lead to a significant strain modulation in both the buffer layer and barrier layer. The strain modulation can further contribute to current collapse.

[0005] To address these problems, some have suggested an AlGaN/GaN(or InGaN)/AlGaN double heterostructure design. While these devices show improvement in the low temperature (i.e., about 200 Kelvin) mobility, no improvement has been demonstrated for the room temperature mobility. Building on this, others have proposed a double heterostructure AlGaN/InGaN/GaN field effect transistor (DHFET) fabricated on an insulating SiC substrate. The DHFETs have demonstrated output RF powers as high as 4.3 Watts/millimeter (W/mm) in continuous wave (CW) mode, 6.3 W/mm in a pulsed mode, with a gain compression as low as four decibels. However, these devices have a relatively high level of low frequency noise that may indicate that these devices will have problems in yield and reliability. These problems are due to a large lattice mismatch between GaN, AlN, and InN, resulting in strong piezoelectric effects that significantly impact electrical and optical properties of III-N heterojunction devices.

[0006] As a result, a need exists for a field effect transistor having an increased lifetime and reliability, while exhibiting a reduced level of noise.

SUMMARY OF THE INVENTION

[0007] The invention provides a heterostructure semiconductor device that includes a composite layer between an active layer and a gate. The composite layer includes a strain matching layer and a barrier layer. The strain matching layer reduces an amount of strain

between the barrier layer and the active layer. The composite layer can include additional layers, such as a quantum well layer, and the device can incorporate one or more additional strain matching layers to reduce strain between other layers. Various gate and/or contact configurations are also provided to further improve various aspects of the device performance.

[0008] A first aspect of the invention provides a heterostructure semiconductor device comprising: a substrate; a buffer layer on the substrate; an active layer on the buffer layer, the active layer comprising at least one group III element and N; and a composite layer on the active layer, the composite layer comprising: a strain matching layer over the active layer, the strain matching layer comprising three group III elements and N; and a barrier layer on the strain matching layer, the barrier layer comprising at least one group III element and N.

[0009] A second aspect of the invention provides a field effect transistor comprising: a substrate; a buffer layer on the substrate, the buffer layer comprising AlN; an active layer on the buffer layer, the active layer comprising GaN; and a composite layer over the active layer, the composite layer comprising: a strain matching layer over the active layer, the strain matching layer comprising AlInGaN; and a barrier layer on the strain matching layer, the barrier layer comprising AlGaN.

[0010] A third aspect of the invention provides a field effect transistor comprising: a substrate; a buffer layer on the substrate, the buffer layer comprising AlN; an active layer on the buffer layer, the active layer comprising GaN; and a composite layer, the composite layer comprising: a quantum well layer over the active layer, wherein the quantum well layer comprises InGaN; a strain matching layer on the quantum well layer, the strain matching layer comprising AlInGaN; and a barrier layer on the strain matching layer, the barrier layer comprising AlGaN.

[0011] The illustrative aspects of the present invention are designed to solve the problems herein described and other problems not discussed, which are discoverable by a skilled artisan.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

[0013] FIG. 1 shows a heterostructure semiconductor device according to one embodiment of the invention;

[0014] FIG. 2 shows a chart of the results of a Secondary Ion Mass Spectrometry analysis of the device in FIG. 1;

[0015] FIG. 3 shows a chart of current as a function of voltage for the device in FIG. 1;

[0016] FIG. 4 shows a chart of the transfer characteristics for the device in FIG. 1 in the saturation regime;

[0017] FIG. 5 shows a chart of the transconductance of the device in FIG. 1 in the saturation regime;

[0018] FIG. 6 shows a chart of the gate current of the device in FIG. 1;

[0019] FIG. 7 shows a heterostructure semiconductor device according to a second embodiment of the invention;

[0020] FIG. 8 shows a heterostructure semiconductor device according to a third embodiment of the invention;

[0021] FIG. 9 shows a heterostructure semiconductor device according to a fourth embodiment of the invention;

[0022] FIG. 10 shows a heterostructure semiconductor device according to a fifth embodiment of the invention;

[0023] FIG. 11 shows a heterostructure semiconductor device according to a sixth embodiment of the invention; and

[0024] FIG. 12 shows a heterostructure semiconductor device according to a seventh embodiment of the invention.

[0025] It is noted that the drawings of the invention are not to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0026] It is understood, that for purposes of this description Al means Aluminum, Ga means Gallium, N means Nitrogen, In means Indium, Si means Silicon, O means Oxygen, and C means Carbon. Further, it is understood that "group III elements" comprise the elements Al, Ga, In, Boron (B), and Thallium (Tl).

[0027] The invention provides a heterostructure semiconductor device that includes a composite layer between an active layer and a gate. The composite layer includes a strain matching layer and a barrier layer. The strain matching layer reduces an amount of strain between the barrier layer and the active layer. The composite layer can include additional layers, such as a quantum well layer, and the device can incorporate one or more additional strain matching layers to reduce strain between other layers. Various gate and/or contact configurations are also provided to further improve various aspects of the device performance.

[0028] Turning to the Figures, FIG. 1 shows a heterostructure semiconductor device 10 according to one embodiment of the invention. Device 10 includes a plurality of stacked layers comprising a substrate 12, a buffer layer 14, an active layer 16, and a composite layer 17. Composite layer 17 includes a strain matching layer 18 and a barrier layer 20. It is understood that any of the layers described herein can comprise a short period superlattice, the various layers can comprise epitaxial structures formed using epitaxy, and device 10 can include n-type or p-type channels, as are known in the art. In one embodiment, active layer 16 comprises a quantum well, and buffer layer 14 has a wider band gap than active layer 16. Device 10 is configured to operate as a field effect transistor. As a result, device 10 includes a gate 22 stacked on composite layer 17, and a source contact 24 and a drain contact 26 each stacked on active layer 16. Both strain matching layer 18 and barrier layer 20 contact the sides of source contact 24 and drain contact 26.

[0029] It is understood that while shown having a source contact 24, gate 22, and drain contact 26 configuration, devices having various contact/gate configurations are possible under the invention. For example, gate 22 could comprise multiple gate fingers connected using bridges that comprise, for example, SiO_2. Further, the geometry of the contacts/gates could be such that a round source contact 24 is surrounded by a ring gate 22 and a ring drain 26 that form concentric circles about source contact 24. While the invention is shown and described as a field effect transistor throughout this discussion, it is understood that the invention can be applied to various types of semiconductor devices, including a photodetector, a gated bipolar junction transistor, a gated hot electron transistor, a gated heterostructure bipolar junction transistor, a gas sensor, a liquid sensor, a pressure sensor, a multi-function sensor (e.g., pressure and temperature), a power switching transistor, and a microwave transistor.

[0030] Device 10 can include any type of substrate 12. For example, substrate 12 can comprise sapphire, silicon carbide (SiC), spinel, silicon, bulk GaN, bulk AlN, or bulk AlGaN. Similarly, any type of buffer layer 14 can be used, for example, buffer layer 14 can comprise AlN. Active layer 16 can comprise a binary compound that includes N and an element selected from the group III elements, or a ternary compound that includes N and two elements selected from the group III elements. Strain matching layer 18 can comprise a quaternary layer that includes three group III elements and N. Barrier layer 20 can comprise a binary compound or ternary compound that includes one or two group III elements and N.

[0031] In one embodiment, device 10 comprises a substrate comprising SiC, a buffer layer 14 comprising AlN, an active layer 16 comprising GaN or InGaN, a strain matching layer 18 comprising AlInGaN, and a barrier layer 20 comprising AlGaN. FIG. 2 shows a chart 30 of the results of a Secondary Ion Mass Spectrometry (SIMS) analysis of device 10 having such a configuration. Chart 30 plots concentration 32 (atoms/cm^3) as a function of depth 34 (nanometers (nm)) within device 10. Barrier layer 20 is located at the top of device 10 and is shown to have relatively high, constant concentrations of Al, Ga, and N. At a depth of approximately twenty-five nm 36, strain matching layer 18 begins. Strain matching layer 18 has a substantially higher concentration of In than barrier layer 20 while maintaining relatively high concentrations of Al, Ga, and N. Strain matching layer 18 has a thickness of about 10 nm, so active layer 16 begins at a depth of approximately thirty-five nm 38. Active layer 16 has substantially lower concentrations of both Al and In than strain matching layer 18, while maintaining constant concentrations of Ga and N.

[0032] It is understood that concentrations of the various elements in any layer can remain constant, vary gradually, or vary abruptly both within a layer or at a junction between two layers.

A desired molar ratio can be used to determine a desired quantity of each group III element in a particular layer. For example, when a ternary compound such as AlGaN is to be used, the ternary compound can be expressed as $Al_xGa_{1-x}N$. In other words, the molar ratio of the two group III elements is such that for every x moles of Al, there are 1-x moles of Ga, where $0<x<1$. Similarly, when a quaternary compound such as AlGaInN is to be used, the quaternary compound can be expressed as $Al_xGa_yIn_{1-x-y}N$. That is, for every mole of group III elements, x moles are Al, y moles are Ga, and 1-x-y moles are In, wherein $0<x<1$, $0<y<1$, and $x+y<1$.

[0033] Returning to FIG. 1, to test device 10, a gate 22 having a length of about 1.5 microns was placed on composite layer 17 (i.e., barrier layer 20), and a source contact 24 and a drain contact 26 were placed on active layer 16 about five microns apart. FIG. 3 shows a chart 40 of device current as a function of device voltage for various grid voltages applied to device 10, FIG. 4 shows a chart 42 of the transfer characteristics (i.e., device current as a function of voltage) for device 10 in the saturation current regime, FIG. 5 shows a chart 44 of the transconductance (i.e., device output current as a function of input voltage) of device 10 in the saturation current regime, and FIG. 6 shows a chart 46 of the gate current of device 10. As can be seen from FIGS. 3-6, device 10 exhibited superior performance than prior art devices having a similar gate length. In particular, device 10 has an excellent linearity (e.g., a very small variation of the device transconductance in the gate voltage range from – 2 V to 2 V), a small knee voltage, and a small gate leakage current.

[0034] Several variations can be made to device 10. For example, FIG. 7 shows a device 110 that includes a plurality of stacked layers comprising a substrate 112, a buffer layer 114, an active layer 116, and a composite layer 117. In this embodiment, composite layer 117 includes a barrier layer 120, a strain matching layer 118, and a quantum well layer 150. Quantum well

layer 150 can comprise a ternary compound that includes two group III elements and N. The inclusion of quantum well layer 150 provides an improved carrier localization. In one embodiment of device 110, buffer layer 114 comprises AlN, active layer 116 comprises GaN or InGaN, quantum well layer 150 comprises InGaN, strain matching layer 118 comprises AlInGaN, and barrier layer 120 comprises AlGaN.

[0035] FIG. 8 shows another device 210 according to still another embodiment of the invention. Device 210 includes a second strain matching layer 252 on an active layer 216 and below a composite layer 217. The presence of second strain matching layer 252 provides additional control over polarization charges in device 210. Second strain matching layer 252 contacts the bottom layer of composite layer 217, i.e., quantum well layer 250. Second strain matching layer 252 can comprise a quaternary layer that includes three group III elements and N, for example, AlGaInN. In this embodiment, a source contact 224 and a drain contact 226 are shown placed on second strain matching layer 252 instead of directly contacting active layer 216.

[0036] FIG. 9 shows another device 310 according to still another embodiment of the invention. Device 310 is configured to operate as a field effect transistor having a recessed gate 322 structure/stack. The recessed gate 322 configuration allows for improved control of strain and electric field distribution near the edges of gate 322. As a result, strain and trapping effects near the edges of gate 322 are reduced. The recessed gate 322 structure can be formed, for example, by removing portions of barrier layer 320 and strain matching layer 318 that are located between gate 322 and a source contact 324, and between gate 322 and a drain contact 326. Alternatively, a mask can be used to prevent barrier layer 320 and/or strain matching layer 318 from being deposited on certain areas of device 310. As shown, barrier layer 320 and strain matching layer 318 can include portions 325, 327 that contact source contact 324 and/or drain

contact 326, respectively. However, the portions of barrier layer 320 and strain matching layer 318 below gate 322 do not contact these portions 325, 327.

[0037] FIG. 10 shows another device 410 that includes a dielectric layer 454 stacked on composite layer 417 (i.e., barrier layer 420), and has a gate 422 placed on dielectric layer 454. By incorporating dielectric layer 454, the amount of leakage current that passes through gate 422 is substantially reduced. Dielectric layer 454 can include Si, and can comprise one or more layers of, for example, SiO_2, and/or SiN. Further, dielectric layer 454 can comprise a ferroelectric layer.

[0038] FIG. 11 shows another device 510 configured to operate as a field effect transistor in which a gate 522 is positioned such that the distance from gate 522 to a source contact 524 is less than the distance from gate 522 to a drain contact 526. By configuring device 510 in this manner, the breakdown voltage for device 510 is increased. Various other gate 522/source contact 524 configurations are possible. For example, the distance from gate 522 to source contact 524 can be zero, and gate 522 can at least partially overlap source contact 524.

[0039] Finally, FIG. 12 shows another device 610 in which the offset gate shown in FIG. 11, and the recessed gate shown in FIG. 9 are combined. By configuring device 610 in this manner, both a larger breakdown voltage and increased reliability are obtained. While the various alternatives are shown incorporating certain alterations and combinations of alterations, it is understood that any combination of the various alterations discussed and other alterations can be incorporated in devices under this invention.

[0040] The foregoing description of various embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are

possible. Such modifications and variations that may be apparent to a person skilled in the art are intended to be included within the scope of the invention as defined by the accompanying claims.